



Altera Quartus II Software v11.1 — Subscription Edition vs. Web Edition

Categories	Features	Web Edition Software	Subscription Edition Software
General Information	Getting started	Download (www.altera.com/download) and DVD	(www.altera.com/dvdrequest)
	Operating system support	Windows: Vista (32 bit), XP (32 bit), 7 (32 bit) Linux: SUSE Linux Enterprise 11 (32 bit), Red Hat Enterprise Linux 4 and 5 (32 bit) CentOS 4 and 5 (32 bit)	Windows: Vista (32/64 bit), XP (32/64 bit), 7 (32/64 bit) Linux: SUSE Linux Enterprise 11 (32/64 bit), Red Hat Enterprise Linux 4 and 5 (32/64 bit) CentOS 4 and 5 (32/64 bit)
Device Support	CPLD	MAX [®] series devices: All	MAX series devices: All
	Low-cost FPGAs	Cyclone [®] V FPGAs: All (Excluding the highest densities) Cyclone IV E/GX FPGAs: All Cyclone III/III LS FPGAs: All Cyclone II FPGAs: All Cyclone FPGAs: None	Cyclone V FPGAs: All Cyclone IV E/GX FPGAs: All Cyclone III/III LS FPGAs: All Cyclone II FPGAs: All Cyclone FPGAs: All
	Mid-range FPGAs	Arria [®] GX FPGAs: None Arria II GX FPGAs: EP2AGX45 Arria V GX FPGAs: None	Arria GX FPGAs: All Arria II GX FPGAs: All Arria V GX FPGAs: All
	High-end FPGAs	Stratix [®] series devices: None	Stratix series devices: All
	ASIC	HardCopy [®] series: None	HardCopy [®] series: All
Intellectual Property (IP)	Altera and partner IP	Yes, including free OpenCore Plus evaluation feature	
	Full-license IP base suite	IP available for purchase	DSP: FIR, FFT, and NCO compilers Interfaces: SerialLite II Memory controllers: DDR1/2/3, QDR II, RDRAM II
Design Entry	Qsys and SOPC Builder	Yes	
	Schematic entry and language support	Schematic entry, Verilog, VHDL, and SystemVerilog	
Design Environment	Tcl scripting , command line support	Yes	
Implementation and Optimization	Incremental compilation and team-based design	No	Yes
	LogicLock [™] incremental design capability	No	Yes
	Multiprocessor support	No	Yes
	Rapid Recompile	No	Yes
	Physical synthesis optimizations	Yes	
	Chip Planner	Yes	
	Live I/O checking	Yes	
	TimeQuest timing analyzer and optimization advisor	Yes	
	Synopsys Design Constraint (SDC) format support	Yes	
	Early power estimator	Available to download on www.altera.com for no cost	
PowerPlay power analysis and optimization	Yes		
Verification and Debug	SignalTap [™] II logic analyzer	Available with TalkBack enabled	Yes
	SignalProbe feature	Available with TalkBack enabled	Yes
	Transceiver Toolkit	No	Yes
	ModelSim [®] -Altera [®] Starter Edition	Included	
	ModelSim-Altera Edition	Sold as an option for \$945	
	Embedded logic analyzer interface	Yes	
	RTL viewer and technology map viewer	Yes	
	Pin planner	Yes	
System Design Software	Nios [®] II Embedded Design Suite	Included in both versions of the Quartus [®] II software	
	DSP Builder	Sold as an option for both versions of Quartus II software	
Third-Party Support	EDA partners	Altera offers third-party support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification	

